Sub-1GHz

©

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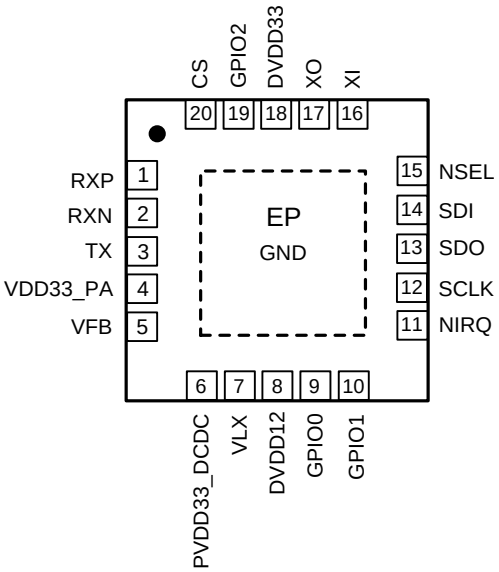
- 20-Pin QFN
- 30MHz

1. 3



1-2 QFN20

Pin	Pin Name	I/O	Description
1	RXP	I	
2	RXN	I	
3	TX	O	
4	VDD33_PA	VDD	PA
5	VFB	I	1.5V 4

©

2

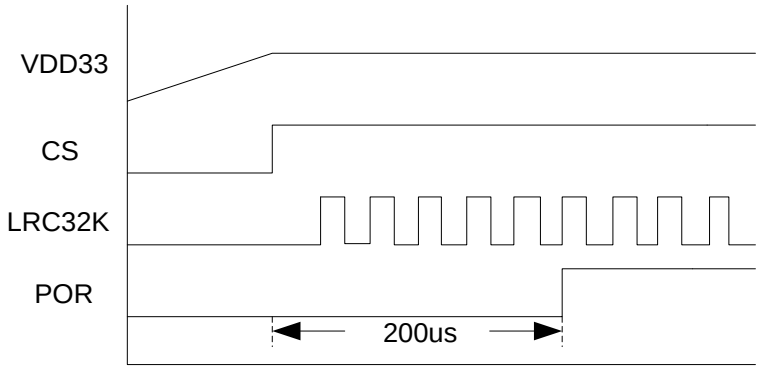
ESW1032 TDD
2 4-FSK/GFSK Sigma-Delta ADC

SPI 256 RX FIFO
MCU

ESW1032 FSK
ESW1032 PA +20 dBm

2. 1 POR

ESW1032 MCU CS LRC32K
5T T LRC POR 3.3V
5T POR



2-1 POR

2. 2 LRC

RC ″H G~

©

©

3

©

SLEEP CMD_READY WUT_UP

GPIO1 /ST_STATE[0]
STARTUP

CMD_READY

3. 3 READY/IDLE

SHUT DOWN IDLE

IDLE SPI SPI
CMD_TXSTR CMD_RXSTR

3. 4 TX

SPI CMD_TXSTR

TX SPI CMD_PDPLL IDLE

3. 5 RX

SPI CMD_RXSTR

RX SPI CMD_PDPLL IDLE

3. 6 WAIT_CMD

WAIT_CMD

WAIT_CMD SPI CMD_TXSTR CMD_RXSTR CMD_PDPLL
IDLE

3. 7

SPI

	SPI
CMD_SLEEP	8'hA0
CMD_READY	8'hA2
CMD_TXSTR	8'hB2
CMD_RXSTR	8'hB3
CMD_PDPLL	8'hB4

3-1

©

3. 8

ESW1032 Sleep READY/IDLE TX RX
SPI CTS CTS

CTS SPI MCU CTS
GPIO1 CTS ST_CTS(SYS 0x1F)

	SHUT DOWN	SLEEP	READY/IDLE	TX	RX
SHUT DOWN			1.31ms	1.49ms	1.47ms
SLEEP			1.44ms	1.62ms	1.60ms
READY/IDLE			s4	180 ms	

0 7 8 9

©

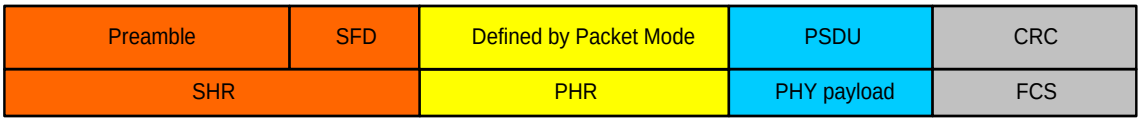
4

ESW1032 GPIO WM-Bus MDM_MODE DATA_MODE

4. 1

IEEE 802.15.4 SUN FSK

MDM_MOD(MDM 0x00) DATA_MODE “ 2'b10 ”



4-1

◆ Preamble

PRMB_LEN0(MDM 0x05) PRMB_LEN1(MDM 0x06) 4~1023 PREAMBLE(MDM 0x04)

◆ SFD

SFD SHR PHR IEEE 802.15.4 SUN FSK SFD FEC

◆ PHR

PHR

◆ PSDU

◆ FCS

FCS 16bits/32bits CRC

4. 1. 1 IEEE 802.15.4 SUN FSK

IEEE 802.15.4 SUN FSK MDM_MOD PACKET_SEL “ IEEE 802.15.4 SUN FSK 2'b10 ”

IEEE 802.15.4 SUN FSK

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◆ PHR

PHR MS REV FCS DW Frame Length 5

‘ MS(Mode Switch)

0 Data Rate Modulation

‘ REV(Reserved)

0

‘ FCS(FCS Type)

IEEE 802.15.4 SUN FSK 4- FCS 2- FCS FEC_CTRL(MDM 0x01) CRC_SIZE CRC FCS Type 4- FCS FCS Type 0 2- FCS FCS Type 1

‘ DW(Data Whitening)

PSDU Data Whitening FEC_CTRL(MDM 0x01) WHITEN_EN Data Whitening Data Whitening Data Whitening 1 0

‘ Frame Length

LSB PSDU_LEN0(MDM 0x15) PSDU_LEN1(MDM 0x16) PSDU Frame Length

◆ PSDU

PSDU FIFO

◆ FCS

FCS 16bits/32bits CRC

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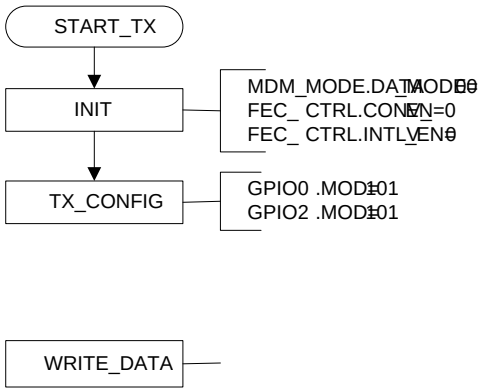
4. 2 GPIO

GPIO MDM_MOD(MDM 0x00) DATA_MODE “ GPIO 2'b00 ”

GPIO0(SYS 0x09) GPIO2(SYS 0x0C) MOD AF1 3'b101 GPIO0 GPIO2

GPIO0(SYS 0x09) GPIO2(SYS 0x0C) MOD AF0 3'b100 GPIO0 GPIO2



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4. 3 WM-Bus

WM-Bus MDM_MOD(MDM 0x00) DATA_MODE “ 2'b10 ” PACKET_SEL “ WM-Bus 2'b11

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5-2 SPI

5-3 SPI

5. 1. 2 SPI

SPI “ Mode Byte ” “ CMD Byte ”

Name	Mode Byte	CMD Byte	Notes
Sleep	8'h80 HV CMD	8'hA0	Command for the SLEEP mode
Ready		8'hA2	Command for the REDAY mode
TXSTR	8'h80 LV CMD	8'hB2	Command to start the TX Modem
RXSTR		8'hB3	Command to start the RX Modem
PDPLL		8'hB4	Command to enter MODEM IDLE

5-1 SPI

5. 2

ESW1032 nIRQ LOW = 0

MCU

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MCU nIRQ
nIRQ

SYS MDM MAC

- SYS
  - LRC
  - RXFIFO
  - RXFIFO
  - TXFIFO
  - TXFIFO
- MDM
  - RX
  - RX MAC
  - RX Payload
  - RX PHR
  - RX
  - TX
- MAC
  - HOP END
  - END_BDI
  - NXT_BI
  - NXT_UDI

IER_SYS IER_MDM IER_MAC
/ nIRQ
IFM_SYS IFM_MDM IFM_MAC

1 0

5. 3 GPIO < J

©

6

6. 1

’0’ ’1’ PN9

PN9 9’h1FF

P(x) = 1+x5+x9

6-1 PN9

IEEE 802.15.4 SUN FSK PSDU+FCS

“ ”

FEC_CTRL(MDM 0x01) WHITEN_EN

PN9_INIT0~PN9_INIT1 (MDM 0x30-0x31)

6. 2 CRC

IEEE 802.15.4 SUN FSK CRC PSDU CRC16/32

FCS16/32

IEEE 802.15.4 SUN FSK CRC

- CRC16 G16(x) = 1+x5+x12+x16
- CRC32 G32(x)= 1+x+x2+x4+x5+x7+x8+x10+x11+x12+x16+x22+x23+x26+x32

FEC_CTRL (MDM 0x01) CRC_EN CRC CRC_SIZE

CRC SIZE

, ³$ À R RĐ "pĐ / À R

©

FEC

FEC

FEC PTX PRX

6. 4

ESW1032 ONEMS (SYS 0x10) 1

CHI_CTL (MAC 0x00) EN_UDI 1 UDI_SET (MAC 0x01)

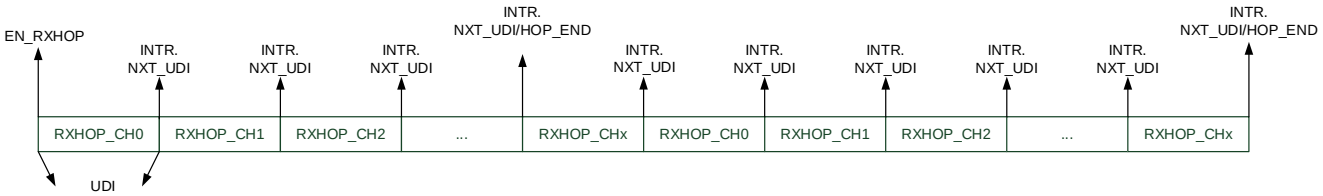
n n-1 CHAN_SPC0 ~ CHAN_SPC1 (MAC 0x4A – 0x4B)

ESW1032 64 RXHOP_CH0 ~ RXHOP_63 RXHOP_CTL (MAC 0x4C) HOP_CHUM

RXHOP_CTL (MAC 0x4C) EN_RXHOP RXHOP_IDX (MAC 0x4D)

RXHOP_CTL (MAC 0x4C) EX_AUTOHOP

64 HOP_END RXHOP_CH0 ~ RXHOP_63 RXHOP_CH0



6-2

STAY_CHAN (MAC 0x4E)

SELF_CHAN (MAC 0x4F)

6. 5 RSSI

ESW1032 RSSI RSSI

-127dBm 0dBm ± 1dB

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7

7. 1

7. 1. 1

7. 1. 1. 1 LRC (LRC_CTL0)

	LRC_CTRL0				
	0x02				
	0x50				
				1	0
TRIM_ENABLE	7:4	W	LRC	1100:	
STATE	7	R	LRC		
-	6	-	-	-	
FAIL	5	R	LRC		
NOTEQU	4	R	LRC		

©

7. 1. 1. 2 GPIO0 (GPIO0)

<table>
<tr><td></td><td colspan="5">GPIO0</td></tr>
<tr><td></td><td colspan="5">0x09</td></tr>
<tr><td></td><td colspan="5">0x00</td></tr>
<tr><td></td><td></td><td></td><td></td><td>1</td><td>0</td></tr>
<tr><td>DI</td><td>7</td><td>R</td><td>GPIO</td><td colspan="2">I/0</td></tr>
<tr><td>-</td><td>6:5</td><td>-</td><td>-</td><td colspan="2">-</td></tr>
<tr><td>PUD</td><td>4:3</td><td>R/W</td><td>/</td><td colspan="2">00 /
01
10
11</td></tr>
<tr><td>MOD</td><td>2:0</td><td>R/W</td><td>GPIO</td><td colspan="2"><table>
<tr><th>Name</th><th colspan="3">Value</th><th>Description</th></tr>
<tr><td>TRISTATE</td><td>0</td><td>0</td><td>0</td><td>/</td></tr>
<tr><td>OUT DRIVE0</td><td>0</td><td>0</td><td>1</td><td>CMOS</td></tr>
<tr><td>OUT DRIVE1</td><td>0</td><td>1</td><td>0</td><td>CMOS</td></tr>
<tr><td>INPUT</td><td>0</td><td>1</td><td>1</td><td>-</td></tr>
<tr><td>AF0</td><td>1</td><td>0</td><td>0</td><td>DEMVALID</td></tr>
<tr><td>AF1</td><td>1</td><td>0</td><td>1</td><td>MODVALID</td></tr>
<tr><td>AF2</td><td>1</td><td>1</td><td>0</td><td>-</td></tr>
<tr><td>AF3</td><td>1</td><td>1</td><td>1</td><td>HOSC_CLK</td></tr>
</table></td></tr>
</table>

7-2 GPIO0

©

7. 1. 1. 4 GPIO2 (GPIO2)

	GPIO2				
	0x0C				
	0x00				
				1	0
DI	7	R	GPIO	I/0	
-	6:5	-	-	-	
PUD	4:3	R/W	/	00 / 01 10 11	

Name	Value			Description
TRISTATE	0	0	0	/
OUT	0	0		

DRIVE0

MOD 2:0 R/W GPIO

©

7. 1. 1. 6 1ms (ONEMS)

	ONEMS				
	0x10				
	0x00				
				1	0
-	7:1	-	-	-	
ONEMS_EN	0	R/W	1ms		

7-6

©

7. 1. 1. 9 (WUT_CNTH)

	WUT_CNTH				
	0x13				
	0x00				
				1	0
WUT_CNTH	7:0	R/W		0~255	

7-9 WUT_CNTH

WUT_EN

7. 1. 1. 10

©

7. 1. 1. 12 MAC (IER_MAC)

	IER_MAC				
	0x16				
	0x00				
				1	0
-	7:4	-	-	-	
HOP_END	3	W			
END_BDI	2	W			
NXT_BI	1	W			
NXT_UDI	0	W			

7-12 IER_MAC

7. 1. 1. 13 (IFM_SYS)

	IFM_SYS				
	0x17				
	0x00				
				1	0
WUT	7	R			
LRC_TRIM	6	R	LRC		
-	5:4	-	-	-	
RXFIFO_ALFULL	3	R	RX FIFO		
RXFIFO_ALEMPTY	2	R	RX FIFO		
TXFIFO_ALFULL	1	R	TX FIFO		
TXFIFO_ALEMPTY	0	R	TX FIFO		

7-13 IFM_SYS

7. 1. 1. 14 MDM (IFM_MDM)

	IFM_MDM				
	0x18				
	0x00				
				1	0
-	7:6	-	-	-	-
RX_PRE_DONE	5	R	RX PRE		

RX

©

7. 1. 1. 15 MAC (IFM_MAC)

	IFM_MAC				
	0x19				
	0x00				
				1	0
-	7:4	-	-	-	-
HOP_END	3	R			
END_BDI	2	R	Ꮁ		Ꮂ

©

©

7. 1. 1. 19 CTS (ST_CTS)

	ST_CTS				
	0x1F				
	0xFF				
				1	0
CTS_VALUE	7:0	R	CTS	0xFF	SPI

7-19 ST_CTS

7. 1. 1. 20 FIFO (FIFO_CTL)

	FIFO_CTL
	0x20

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7. 1. 1. 27 LRC (LRC_CNTL)

	LRC_CNTL				
	0x7E				
	0x00				
				1	0
LRC_CNTL	7:0	R	LRC	LRC	

7-27 LRC_CNTL

7. 1. 1. 28 LRC (LRC_CNTH)

	LRC_CNTH				
	0x7F				
	0x00				
				1	0
CAP_TRIM_BYP	7	R/W	LRC CAP BYPASS	CAP	CAP
-	6:3	-	-	-	-
SIGN	2	R	LRC		
LRC_CNTH	1:0	R	LRC		

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7. 1. 2 MODEM

7. 1. 2. 1 (MDM_MODE)

	MDM_MODE				
	0x00				
	0x00				
				1	0
4FSK_EN	7	R/W	4FSK		
GFSK_EN	6	R/W	GFSK		
-	5	-	-	-	-
PAYLOAD_MODE	4	R/W		LSB	MSB
PACKET_SEL	3:2	R/W		00 /01: 10 :IEEE 802.15.4 SUN FSK 11 : WM-Bus	
DATA_MODE	1:0	R/W		00 :GPIO 01 : 10 : 11:	

7-29 MDM_MODE

7. 1. 2. 2 (PREAMBLE)

	PREAMBLE

0x04 8 >6(15.48.76 1.44 1(A)6MCID 58 >615.48 r_0 1 T

©

7. 1. 2. 4 1 (PRMB_LEN1)

	PRMB_LEN 1				
	0x06				
	0x00				
				1	0
-	7:3	-	-	-	-
PRMB_LEN1	2:0	R/W	Preamble [10:8]	WM_Bus	Byte

7-32 PRMB_LEN1

7. 1. 2. 5 0 (SFD0)

	SFD0				
	0x07				
	0x00				
				1	0
SFD0	7:0	R/W	SFD [7:0]	SFD	1 Byte

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7. 1. 2. 12 7 (SFD7)

	SFD7				
	0x0E				
	0x00				
				1	0
SFD7	7:0	R/W	SFD [31:24]	SFD 4	Byte

7-40 SFD7

7. 1. 2. 13

©

7. 1. 2. 16 (RX_PSDU_LEN0)

	RX_PSDU_LEN0				
	0x1A				
	0x00				
				1	0
RX_PSDU_LEN0	7:0	R	[7:0]	Byte	

7-44 RX_PSDU_LEN0

7. 1. 2. 17 (RX_PSDU_LEN1)

	RX_PSDU_LEN1				
	0x1B				
	0x00				
				1	0
-	7:4	-	-	-	-
RX_PSDU_LEN1	3:0	R	[11:8]	Byte	

7-45 RX_PSDU_LEN1

7. 1. 2. 18 PHR0 (PHR0_STS)

	PHR0_STS				
	0x1C				
	0x00				
				1	0
PHR0_STS	7:0	R	PHR[7:0]	PHR	1

7-46 PHR0_STS

7. 1. 2. 19 PHR1 (PHR1_STS)

	PHR1_STS				
	0x1D				
	0x00				
				1	0
PHR1_STS	7:0	R	PHR[15:8]	PHR	2

7-47 PHR1_STS

©

7. 1. 2. 20 PHR2 (PHR2_STS)

	PHR2_STS				
	0x1E				
	0x00				
				1	0
PHR2_STS	7:0	R	PHR[23:16]	PHR	3

7-48 PHR2_STS

7. 1. 2. 21 PHR3 (PHR3_STS)

	PHR3_STS
	0x1F
	0x00

1 0

©

7. 1. 2. 24 RSSI 0 (RSSI0)

	RSSI0				
	0xD6				
	0x00				
				1	0
RSSI0	7:0	R	RSSI [7:0]		

7-52 RSSI0

7. 1. 2. 25 RSSI 1 (RSSI1)

	RSSI1				
	0xD7				
	0x00				
				1	0
RSSI1	7:0	R	RSSI [7:0]		

7-53 RSSI1

©

7. 1. 3. 4 (SYNC_UDI_CNT)

	SYNC_UDI_CNT				
	0x26				
	0x00				
				1	0
SYNC_UDI_CNT	7:0	R	[7:0]		

7-57 SYNC_UDI_CNT

7. 1. 3. 5 0 (CHAN_SPC0)

	CHAN_SPC0				
	0x4A				
	0x00				
				1	0
CHAN_SPC0	7:0	R/W	[7:0]	0	

7-58 CHAN_SPC0

7. 1. 3. 6 1 (CHAN_SPC1)

	CHAN_SPC1				
	0x4B				
	0x00				
				1	0
CHAN_SPC1	7:0	R/W	[15:8]	1	

7-59 CHAN_SPC1

7. 1. 3. 7 (RXHOP_CTL)

©

1

	Vdd	-	1.8	3.3	3.6	V
	Temp_W	-	-40	27	85	
	-	-	-	1	-	m Y V
:						
1.						

7-65

	Vdd	-	-0.3	3.6	V
	Vin	-	-0.3	3.6	V
	Tj	-	-40	125	
	Tstg	-	-50	150	
	Tsdr	30	-	255	
ESD	-	HBM	-2	2	kV
	-	85	-350	350	mA

:

1.

2. ESD

ESD

3. PIN3

ESD 350 8

©

		+13 dBm	433MHz	-	44	-	mA
		+13 dBm	868MHz	-	47	-	mA

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@433MHz	IMR433	DR = 2.4kbps; FDEV = 1.2kHz; BW=6 kHz; CW				

©

	Ttune	-	-	150	-	us
	F_{PLL}	PL_BANDSEL[2:]=5	142	–	175	MHz
		PL_BANDSEL[2:]=4	210	–	262	MHz
		PL_BANDSEL[2:]=3	284	–	350	MHz
		PL_BANDSEL[2:]=2	420	–	525	MHz
		PL_BANDSEL[2:]=0	850	–	1050	MHz
	$F_{RES-960}$	F_{PLL}=850-1050 MHz	–	28.6	–	Hz
	$F_{RES-525}$	F_{PLL}=420-525 MHz	–	14.3	–	Hz
	$F_{RES-350}$	F_{PLL}=284-35.7m [(=2)-5(8)]TJ 038c 0 T<w-0F216407033<)3< -EMC1< 86=<9M<3D062				

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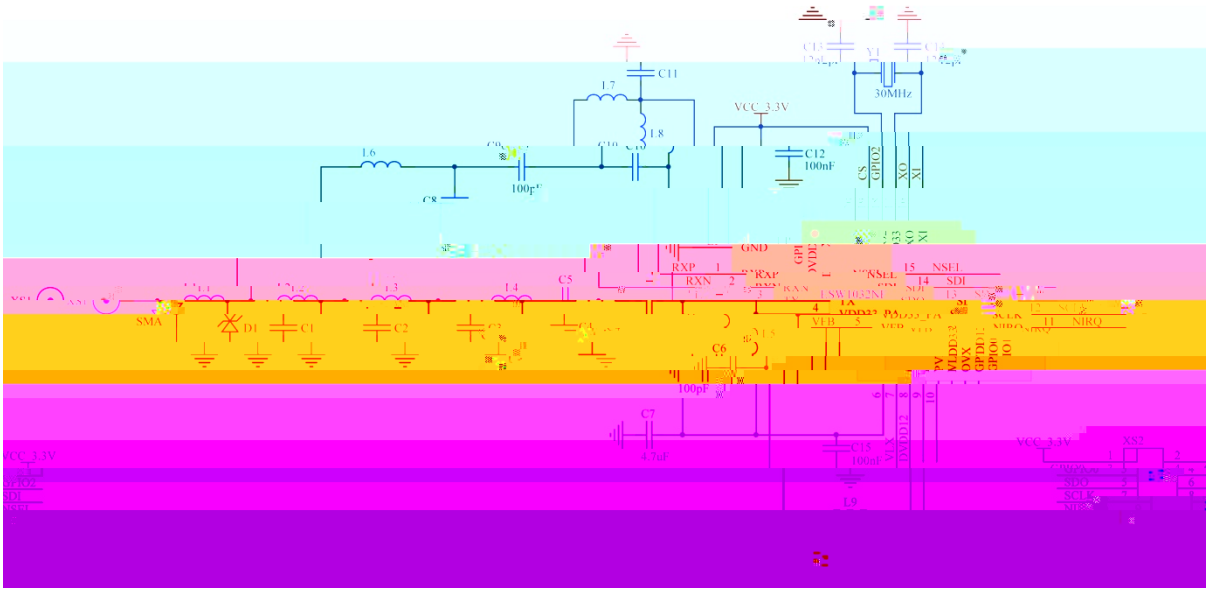
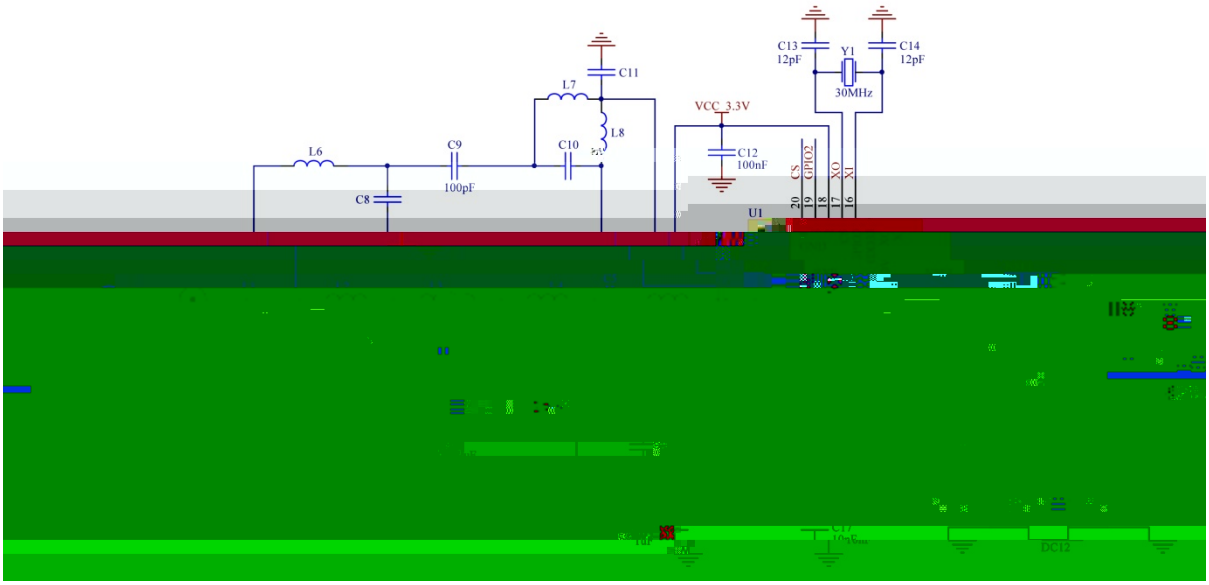
2



7-1 DC/DC ON



7-2 DC/DC OFF

AN1077_ _ESW1032_Hardware_Reference_Design

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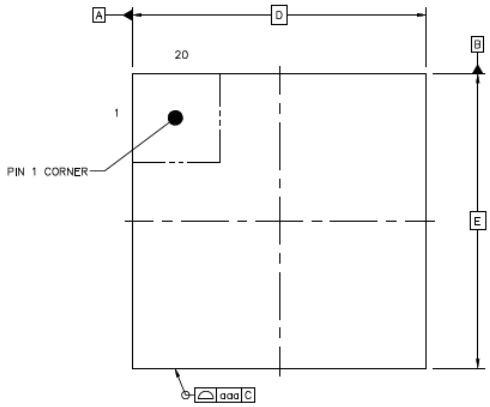
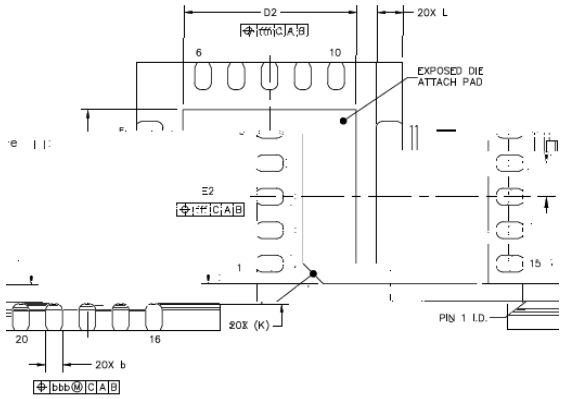
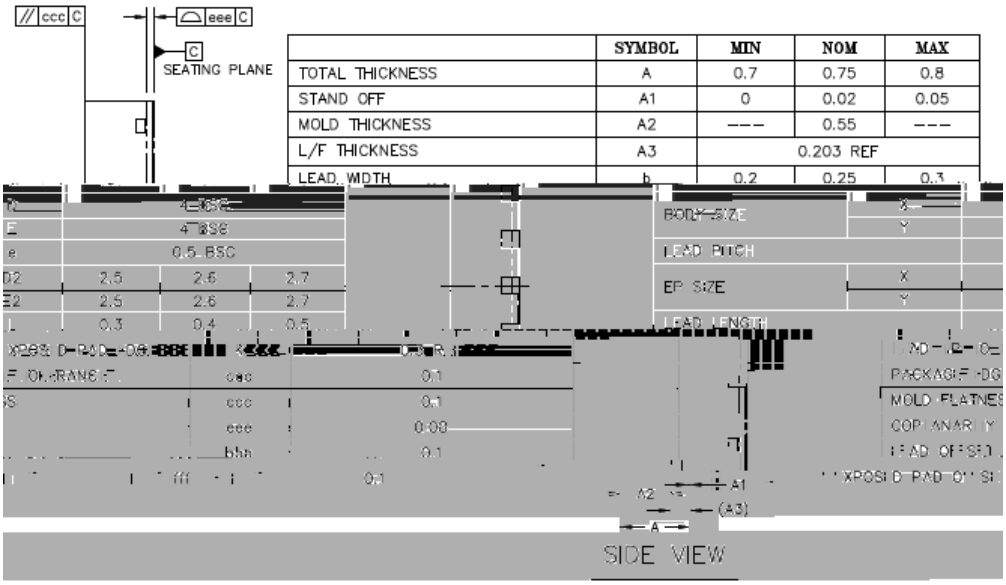
3



TOP VIEW



BOTTOM VIEW



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3	0.203 REF		
LEAD WIDTH	b	0.2	0.25	0.3
BODY SIZE	X			
	Y			
LEAD PITCH				
EP SIZE	X			
	Y			
LEAD LENGTH				
PACKAGE EDGE TOLERANCE	aaa		0.1	
	ccc		0.1	
MOLD FLATNESS	eee		0.08	
COPLANARITY	bbb		0.1	
LEAD OFFSET			0.1	
EXPOSED PAD OFFSET				

7-3 QFN20

MM

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